WHAT IS CLAIMED IS:

- 1 1. A method of refreshing memory cells in a memory array, the method comprising:
- 2 receiving an indication that the memory array is to perform a refresh operation, wherein
- 3 the refresh operation comprises at least two refresh cycles, each refresh cycle having an
- 4 activation interval followed by a precharge interval;
- 5 initiating a first refresh cycle by activating a first wordline coupled to a first group of
- 6 memory cells, each memory cell in the first group of memory cells in electrical communication
- 7 with a sense amplifier in a first group of sense amplifiers;
- 8 initiating a second refresh cycle by activating a second wordline coupled to a second
- 9 group of memory cells, each memory cell in the second group of memory cells in electrical
- 10 communication with a sense amplifier in a second group of sense amplifiers where no sense
- amplifier in the first group is in the second group and no sense amplifier in the second group is in
- the first group, and wherein the second refresh cycle is initiated at least a current surge time after
- the initiation of the first refresh cycle but prior to the completion of the first refresh cycle.
- 1 2. The method of claim 1 wherein the second refresh cycle is initiated during the precharge
- 2 interval of the first refresh cycle.
- 1 3. The method of claim 1 wherein the second refresh cycle is initiated during the activation
- 2 interval of the first refresh cycle.
- 1 4. The method of claim 1 and further comprising selectively generating first and second row
- 2 addresses to activate the first and second wordlines such that each sense amplifier in the second

- 3 group of sense amplifiers is electrically isolated from each memory cell in the first group of
- 4 memory cells.
- 1 5. The method of claim 4 wherein a refresh controller selectively generates the first and
- 2 second row addresses.
- 1 6. The method of claim 4 wherein an address generator selectively generates the first and
- 2 second row addresses.
- 1 7. The method of claim 4 wherein a row decoder accepts an input signal from an address
- 2 counter and selectively generates the first and second row addresses.
- 1 8. The method of claim 1 and further comprising initiating the first refresh cycle by
- 2 activating a first plurality of wordlines controlling the first group of memory cells, the plurality
- 3 of wordlines coupled to a plurality of rows to be simultaneously refreshed.
- 1 9. The method of claim 8 and further comprising initiating the second refresh cycle by
- 2 activating a second plurality of wordlines controlling the second group of memory cells, each
- 3 memory cell in the second group of memory cells in electrical communication with a sense
- 4 amplifier electrically isolated from each memory cell in the first group of memory cells.
- 1 10. The method of claim 1 wherein receiving an indication comprises receiving an indication
- 2 to refresh a plurality of rows of memory cells, the plurality of rows of memory cells being fewer
- 3 than all of the rows of memory cells.

- 1 11. The method of claim 10 wherein receiving an indication comprises receiving an
- 2 indication to refresh a plurality of rows of memory cells, the plurality of rows of memory cells
- 3 being at least four rows but no more than sixteen rows.
- 1 12. The method of claim 1 wherein receiving an indication comprises receiving an indication
- 2 to refresh every memory cell in the memory array.

- 1 13. A dynamic random access memory array comprising:
- a plurality of blocks of memory cells, each block including a plurality of rows and
- 3 columns of memory cells;
- a plurality of banks of sense amplifiers wherein each bank of sense amplifiers is located
- 5 between adjacent blocks of memory cells such that each sense amplifier is coupled to columns of
- 6 memory cells in two adjacent blocks;
- 7 a row decoder coupled to each of the blocks of memory cells, the row decoder having a
- 8 plurality of control outputs, each of the control outputs coupled to a row of memory cells; and
- a refresh controller adapted to generate a row address sequence for a plurality of refresh
- 10 cycles, each of the refresh cycles having an activation interval followed by a precharge interval,
- wherein a first refresh cycle of a row in a first one of the blocks is followed by a second refresh
- cycle in a row in a second one of the blocks, the first block not being adjacent to the second
- block, wherein the refresh controller causes the second refresh cycle to be initiated at least a
- surge time after the initiation but prior to the completion of the first refresh cycle.
- 1 14. The memory device of claim 13 wherein the refresh controller causes the second refresh
- 2 cycle to be initiated during the precharge interval of the first refresh cycle.
- 1 15. The memory device of claim 13 wherein the refresh controller causes the second refresh
- 2 cycle to be initiated during the activation interval of the first refresh cycle.

- 1 16. A method of refreshing a dynamic random access memory array that includes a plurality
- 2 of blocks with rows and columns of memory cells and a plurality of banks of sense amplifiers
- 3 wherein each bank of sense amplifiers is shared between adjacent blocks of memory cells such
- 4 that each sense amplifier is coupled to columns of memory cells in two adjacent blocks, the
- 5 method comprising:
- 6 receiving an indication that the memory array is to perform a self refresh operation,
- 7 wherein the refresh operation comprises a plurality refresh cycles to sequentially refresh all rows
- 8 in the array, each refresh cycle having an activation interval followed by a precharge interval;
- 9 and
- sequentially initiating each of the plurality of refresh cycles by:
- 11 (a) activating a wordline coupled to a row of memory cells in a first one of the
- 12 banks;
- 13 (b) after waiting a period of time less than a refresh cycle time but not less than a
- 14 current surge time, activating a wordline coupled to a row of memory cells in a second one of the
- banks, the second one of the banks not sharing a sense amplifier the first one of the banks; and
- (c) repeating step (b) until each row of memory cells in the array has been
- 17 refreshed.
- 1 17. The method of claim 16 wherein the second refresh cycle is initiated during the precharge
- 2 interval of the first refresh cycle.
- 1 18. The method of claim 16 wherein the second refresh cycle is initiated during the activation
- 2 interval of the first refresh cycle.

- 1 19. The method of claim 16 wherein (a) activating a wordline comprises simultaneously
- 2 activating a plurality of wordlines.
- 1 20. The method of claim 19 wherein the number of wordlines in the plurality of wordlines is
- 2 determined by an amount of current drawn by the memory array during a refresh cycle of a
- 3 single row.

- 1 21. A dynamic random access memory array comprising:
- a plurality of blocks of memory cells, each block including a plurality of rows and
- 3 columns of memory cells;
- a plurality of banks of sense amplifiers wherein each bank of sense amplifiers is located
- 5 between adjacent ones of the blocks of memory cells such that each sense amplifier is coupled to
- 6 columns of memory cells in two adjacent blocks;
- 7 means for receiving an indication that the memory array is to perform a refresh operation,
- 8 wherein the refresh operation comprises at least two refresh cycles, each refresh cycle having an
- 9 activation interval followed by a precharge interval; and
- means for initiating a first refresh cycle of a row in a first one of the blocks followed by a
- second refresh cycle in a row in a second one of the blocks, the first block not being adjacent to
- the second block, wherein means for initiating causes the second refresh cycle to be initiated
- after the initiation of but prior to the completion of the first refresh cycle.
- 1 22. The memory array of claim 21 wherein the means for initiating causes the second refresh
- 2 cycle to be initiated during the precharge interval of the first refresh cycle.
- 1 23. The memory array of claim 21 wherein the means for initiating causes the second refresh
- 2 cycle to be initiated during the activation interval of the first refresh cycle.